ABSTRACT OF THE DISCLOSURE

A hardware-based random number generator is provided for incorporation within an integrated circuit. The random number generator includes a first variable frequency oscillator, a second variable frequency oscillator, and frequency variation logic. The first variable frequency oscillator generates a first oscillatory signal at a first frequency. The second variable frequency oscillator generates a second oscillatory signal that is asynchronous to the first oscillatory signal and has a second frequency less than the first frequency. Bits of the random number are configured from samples of the first oscillatory signal taken at the second frequency. The frequency variation logic is coupled to the second variable frequency oscillator. The frequency variation logic generates a noise signal that directs the second variable frequency oscillator to vary the second frequency. The noise signal corresponds to parity of a third oscillatory signal and a fourth oscillatory signal, where the third and fourth oscillatory signals are asynchronous to each other and to the first and second oscillatory signals.